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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/395,294	09/13/1999	SOPHIE WILSON	1073/OG117	5796

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EXAMINER
DECKTER, STEPHANIE M

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/395,294	WILSON, SOPHIE	
	Examiner	Art Unit	
	Stephanie M. Deckter	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2002 and 01 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

a. Please insert a reference to the United States patent application serial number, 09/395,294, for "co-pending application (GB-9916566.4, entitled An Instruction Set for a Computer)" on page 6 of the specification. Further updated status of this co-pending application, such as pending, abandoned, or patented (with appropriate patent number) is further required as necessary.

b. On the 11th line of the second paragraph of the 9th page of the specification, please change "format (3)" to --format L3-- to correctly reference figure 5.

Appropriate correction is required.

Claim Objections

2. Claims 3 and 8 are objected to in view of Applicant's remarks as part of amendment filed 4/15/02 and supplemental amendment filed 5/1/02, both part of paper number 7, that: "the limitation referred to by the Examiner means that both channels simultaneously execute the same operation. The 'single operation', as set forth in claim 3, refers to a single data set" in the second paragraph of page 5. Upon attributing this meaning to the recitation of claim 3, it becomes contrary to the invention as described in the specification and claim 8, which recites the limitation "when the instruction defines a single operation, controlling the first and second processing channels to cooperate to implement said single operation" (emphasis added) in lines 9 and 10 of the claim. Furthermore, it is unclear as to how and why two channels would both execute the same operation using the same data. This appears to be redundant and a waste of

resources. However, if the two channels simultaneously cooperate to implement the single operation, as claimed in 8, this would be a constructive use of resources as each channel would execute the operation with half the data such that the entire "data set" can be used in half the time. Appropriate correction is required.

3. Claim 12 (as amended) recites the limitation "and each instruction identifies a set fo (sic) identification bits locations within the instruction, said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction" in lines 7-11 of the claim as amended. In view of Applicant's remarks of paper 7 that: "claim 13 has been canceled, and the subject mater thereof has been incorporated into claim 12" on page 4, lines 1-2, it appears that Applicant meant the limitation mentioned above to read "and each instruction includes a set of identification bits at designated bit locations within the instruction, said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction" as originally claimed in 13. Please change this language accordingly. Appropriate correction is required. Furthermore, the claim language of canceled claim 13 will be assumed for examination purposes.

4. Claim 12 (as amended) recites the limitation "a computer program comprising" in the first line of the claim. It appears that Applicant meant to recite "a computer program product comprising" based on the limitation "wherein the computer program product" set forth in line 5 of the claim. Applicant should please note that a computer program is not statutory subject matter and would necessitate a rejection under 35 USC § 101 should claim 12 remain in this condition.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 12~~-13~~ and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Fleck et al., U.S. Patent Number 6,292,845. Referring to claim 12, Fleck has taught a computer program product comprising program code means which include

a. a sequence of instructions (column 2, lines 44-45 and 49-50, figure 1, element 1) all having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3),

b. said instructions including long instructions wherein said predetermined bit length defines a single operation (figure 2, element 219)

c. and dual operation instructions wherein said predetermined bit length defines two independent operations (figure 2, element 206),

d. wherein the computer program product is adapted to run on a computer such that the long instructions control the resources of the computer in a first way, and the dual

operation instructions control the resources of the computer in a second way (column 3, lines 33-38), and

e. each instruction includes a set of identification bits at designated bit locations within the instruction (figure 3a), said identification bits being adapted to cooperate with a decode unit of a computer system (column 2, lines 52-55 and figure 1, element 7) to designate whether the instruction is a long instruction or a dual operation instruction (column 4, line 63 to column 5, line 7).

7. Referring to claim 16, Fleck has taught a computer program product comprising program code means which include

a. a sequence of instructions (column 2, lines 44-45 and 49-50, figure 1, element 1) all having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3),

b. said instructions including long instructions wherein said predetermined bit length defines a single operation (figure 2, element 219)

c. and dual operation instructions wherein said predetermined bit length defines two independent operations (figure 2, element 206),

d. said instructions including a set of identification bits at designated bit locations within the instruction (column 4, line 63 to column 5, line 7 and figure 3a)

e. wherein the computer program product is adapted to run on a computer such that said identification bits are adapted to cooperate with a decode unit of the computer (column 2, lines 52-55 and figure 1, element 7) to designated whether:

i. the instruction is a long instruction or a dual operation instruction (column 4, line 67 to column 5, line 3 and figure 3a, Bit 0); and

ii. in the case of dual operation instruction, the nature of each operation in the instruction selected from a data processing category and a memory access category (column 5, lines 3-7, column 2, lines 12-13 and 18-20 and figure 3a, Bit 1).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 (herein referred to as Fleck) in view of Shiell et al., U.S. Patent Number 6,317,820 (herein referred to as Shiell). Referring to claim 1, Fleck has taught a computer system comprising

a. a decode unit for decoding instructions (column 2, lines 52-55 and figure 1, element 7) fetched from a memory holding a sequence of instructions (column 2, lines 44-45 and 49-50, figure 1, element 1), all instructions in the sequence having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3); and

b. first and second processing channels (column 2, lines 4-5 and figure 1, elements 10 and 11)

c. wherein the decode unit is operable to detect for each instruction of said predetermined bit length whether the instruction defines a single operation or two independent operations (column 4, line 67 to column 5, line 3, figure 1, element 7 and

figure 3a) and to control the first and second channels in dependence on said detection (column 2, lines 55-65).

Fleck has not taught the first and second processing channels where each channel comprises a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit. Shiell has taught first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit (Shiell column 3, lines 54-61 and figure 1, elements 130A and 130B which include elements S1, L1, M1, D1, S2, L2, M2, and D2). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the first and second processing channels of Shiell with the processing channels of Fleck having data processing and memory access units in each channel. Doing so would have been beneficial in that task-level parallelism would have been increased due to the greater number of functional units of the processor (Shiell column 1, lines 16-39).

10. Referring to claim 2, Fleck has taught when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously (column 3, lines 33-39).

11. Referring to claim 5, Fleck has taught the decode unit operable to make said detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction (figure 1, element 7 and column 4, line 63 to column 5, line 7 and figure 3a).

12. Referring to claim 6, Fleck and Shiell have taught each limitation of claim 6, including an instruction having a length of n bits wherein one of the predetermined bit locations include the nth and (n+1)st bit. The other predetermined bit location including the n/2th bit has not been taught. However, changing the predetermined location of the second identification bit from the (n+1)st bit to the n/2th bit would have been an obvious improvement. One of ordinary skill in the art would have been motivated to do so in order to better tag or track information regarding the second operation of the instruction by moving the bit closer to such instruction. Also see In re Japikse, **86 USPQ 70 (CCPA 1950)**.

13. Referring to claim 7, Fleck has taught a decode unit operable to identify certain combinations of said independent operations in an instruction based on said set of identification bits, wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation and a fourth combination denotes a long instruction (column 3, lines 15-24, 33-52, figure 2, column 4, line 63 to column 5, line 7 and figure 3A).

14. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820 and further in view of Mohamed, U.S. Patent Number 6,230,180. Fleck and Shiell have taught each limitation of claim 3, including detection by the decode unit that an instruction defines a single operation (column 4, line 67 to column 5, line 3, figure 1, element 7 and figure 3a) as well as control of the

first and second processing channels by the decode unit (column 2, lines 55-65). The further limitation that the first and second channels each simultaneously execute the single operation has not been taught. Mohamed has taught simultaneous execution of a single instruction with multiple data (column 1, lines 59-64). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the method of simultaneous execution of a single instruction with multiple data within the functional units of the first and second processing channels of Shiell. Doing so would have been beneficial in order to increase data parallelism (Mohamed column 1, lines 64-67) by reducing the size of necessary program memory in that only one copy of the code being simultaneously executed is required, as opposed to a copy for each functional unit.

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820 and further in view of Mukhanov, U.S. Patent Number 5,365,476. Shiell and Fleck have taught each limitation of claim 4, including first and second channels sharing at least one common register file (column 4, lines 24-29 and figure 1, elements 140A and 140B). However, simultaneous access of the register file by the channels has not been explicitly taught. Mukhanov has taught a register file that can be simultaneously accessed by more than one functional unit (Mukhanov column 2, lines 34-43). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the register file of Mukhanov as the register file of Shiell. Doing so would have been beneficial in that a dual read port would save cycles otherwise required for register fetch operations if the register file could only be accessed by one functional unit at a time (Mukhanov column 2, lines 44-47).

16. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820 and further in view of Mohamed, U.S. Patent Number 6,230,180. Referring to claim 8, Fleck has taught a method of operating a computer system which comprises

a. first and second processing channels (column 2, lines 4-5 and figure 1, elements 10 and 11), the method comprising

b. decoding an instruction (column 2, lines 52-55 and figure 1, element 7) having a predetermined bit length (column 2, lines 51-53 and figure 1, element 3) to detect whether that instruction defines a single operation or two independent operations (column 4, line 67 to column 5, line 3, figure 1, element 7 and figure 3a);

c. where the instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously (column 3, lines 33-39)

d. when the instruction defines a single operation, controlling the first and second processing channels (column 2, lines 55-65).

Fleck has not taught the first and second processing channels where each channel comprises a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit. Shiell has taught first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory

access unit (Shiell column 3, lines 54-61 and figure 1, elements 130A and 130B which include elements S1, L1, M1, D1, S2, L2, M2, and D2). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the first and second processing channels of Shiell with the processing channels of Fleck having data processing and memory access units in each channel. Doing so would have been beneficial in that task-level parallelism would have been increased due to the greater number of functional units of the processor (Shiell column 1, lines 16-39). Furthermore, Fleck has not taught the further limitation that the first and second channels cooperate to execute the single operation. Mohamed has taught simultaneous execution of a single instruction with multiple data (column 1, lines 59-64), i.e. cooperation among functional units to execute a single operation. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the method of cooperative execution of a single instruction with multiple data within the functional units of the first and second processing channels of Shiell. Doing so would have been beneficial in order to increase data parallelism (Mohamed column 1, lines 64-67), i.e. a single operation can be executed faster if more than one functional unit operates on the associated data.

17. Referring to claim 9, Fleck has taught the step of decoding and detecting comprises reading the values of a designated set of identification bits at predetermined bit locations in the instruction (column 4, line 63 to column 5, line 7 and figure 3a).

18. Referring to claim 10, Fleck has taught said designated bits are used to denote the nature of independent operations when the instruction defines two operations (column 2, lines 14-15 and 18-20), in addition to designating that the instruction defines a single operation (column 4, line 63 to column 5, line 7 and figure 3a).

19. Referring to claim 11, Fleck has taught an instruction having a length of n bits wherein one of the predetermined bit locations includes the nth bit and the other predetermined bit location includes the (n+1)st bit. The other predetermined bit location including the n/2th bit has not been taught. However, changing the predetermined location of the second identification bit from the (n+1)st bit to the n/2th bit would have been an obvious improvement. One of ordinary skill in the art would have been motivated to do so in order to better tag or track information regarding the second operation of the instruction by moving the bit closer to such instruction. Also see In re Japikse, **86 USPQ 70 (CCPA 1950)**.

20. Claims 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845. Fleck has taught each limitation of claim 14, including an instruction having a length of n bits wherein one of the predetermined bit locations includes the nth bit and the other predetermined bit location includes the (n+1)st bit. The other predetermined bit location including the n/2th bit has not been taught. However, changing the predetermined location of the second identification bit from the (n+1)st bit to the n/2th bit would have been an obvious improvement. One of ordinary skill in the art would have been motivated to do so in order to better tag or track information regarding the second operation of the instruction by moving the bit closer to such instruction. Also see In re Japikse, **86 USPQ 70 (CCPA 1950)**.

21. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fleck et al., U.S. Patent Number 6,292,845 in view of Shiell et al., U.S. Patent Number 6,317,820. Fleck has taught a method of operating a computer system which comprises

a. first and second processing channels (column 2, lines 4-5 and figure 1, elements 10 and 11), the method comprising

i. fetching a sequence of instructions from a program memory (column 2, lines 44-45 and 49-50, figure 1, element 1), all said instructions having the same predetermined bit length (column 2, lines 51-53 and figure 1, element 3) and containing a set of designated bits at predetermined bit locations within said bit length (column 4, line 63 to column 5, line 7 and figure 3a);

ii. decoding each instruction (column 2, lines 52-55 and figure 1, element 7), said decoding step including reading the values of said designated bits to determine:

iii. whether the instruction defines a single operation or two independent operations (column 4, line 67 to column 5, line 3 and figure 3a, Bit 0); and

iv. where the instruction defines two independent operations, the nature of each of those operations selected at least from a data processing category of operation and a memory access category of operation (column 5, lines 3-7, column 2, lines 12-13 and 18-20 and figure 3a, Bit 1).

Fleck has not taught the first and second processing channels where each channel comprises a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit. Shiell has taught first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit (Shiell column 3, lines 54-61 and figure 1, elements 130A and 130B which include elements S1, L1, M1, D1, S2, L2, M2, and D2). It would have been obvious to a person of

ordinary skill in the art at the time the invention was made to replace the first and second processing channels of Shiell with the processing channels of Fleck having data processing and memory access units in each channel. Doing so would have been beneficial in that task-level parallelism would have been increased due to the greater number of functional units of the processor (Shiell column 1, lines 16-39).

22. The rejections are respectfully maintained and incorporated by reference as set forth in the last Office Action, mailed 1/15/02, paper number 6.

Remarks

23. Applicant's arguments filed 4/15/02 and 5/1/02, both part of paper number 7, have been fully considered but are not deemed to be persuasive.

24. In the remarks, Applicant argues on page 6, in substance that:

> "*Fleck*, however, does not teach identification bits that cooperate with a decode unit for determining whether the instruction is a long or a dual operation instruction, as set forth in amended claim 12 and independent claim 16. Instead, the identification bits of *Fleck* cooperate with a type evaluation unit that controls the decision of the instructions through a multiplexer. A type evaluation unit does not have the same functionality as a decoder (i.e., the type evaluation unit does not decode)."

In addition, Applicant further argues this point on page 7, first paragraph, in reference to claim 15. This is not found persuasive because it is well known in the art that the responsibilities of a decode unit include determining the type of instruction presented, i.e. arithmetic, memory, branch, etc., in order to determine which functional unit should receive the instruction during the next stages of the pipeline. Therefore, although Fleck has named his decode unit a "type evaluation unit" it does not prevent this feature from performing the same function as the claimed "decode unit." Furthermore, amended claim 12 and independent claim 16 do not further limit the actual function of the decode unit beyond the limitation that "the identification bits

being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction" which has in fact been taught by Fleck. Please see rejection of claims 12 and 16 above.

25. In the remarks, Applicant argues on page 6, second paragraph, in substance that:

> "*Fleck*, however does not disclose or suggest a decoder with the functionality of controlling the channels or detect the type of instructions, as set forth in independent claim 1. Instead, *Fleck* teaches a type evaluation unit that controls an alignment multiplexer."

This is not found persuasive because Fleck does in fact disclose a decoder, named a type evaluation unit as discussed in the preceding paragraph, to control the channels. Applicant is correct in stating that Fleck teaches a decode unit that controls an alignment multiplexer. The alignment multiplexers then control the two channels as taught in the rejection of claim 1 above. Since the type evaluation unit must control the multiplexers, effectively, the type evaluation unit controls the two channels. In addition, since the language of this claim begins with "a computer system comprising" this extra method step and hardware may exist and still read on the claim. Furthermore, the type evaluation unit does in fact detect the type of instructions, as its name suggests, and as taught above in the rejection of claim 1 and the preceding paragraph.

26. In the remarks, Applicant argues on page 7, middle paragraph, in substance that:

> "... each processing channel in the claimed invention comprises a plurality of functional units. This feature, however, is also not found in *Fleck*, nor is it found in *Sheill* (sic)."

This is not found persuasive because although Applicant is correct that Fleck has not taught each channel having a plurality of functional units, Applicant is mistaken that Shiell has not taught this feature. Shiell has in fact taught plural functional units in each channel in column 3, lines

54-61 and as shown in figure 1 where each of the two sides, or channels, of the processor, labeled 130A and 130B, comprises four functional units, called S, L, M. and D units, respectively.

27. Applicant further agues on page 7, middle paragraph, in substance that:

> "Moreover, a person having the ordinary level of skill in the art would not have been motivated to modify *Fleck* by adding the task-level parallelism found in *Shiell* et al. because, as stated previously, task-level parallelism already exists in *Fleck*."

Applicant is correct that task-level parallelism does already exist in Fleck and therefore has given evidence that parallelism is a key objective of Fleck's invention. Therefore, the fact that Shiell has taught using plural functional units to further increase task-level parallelism would have motivated a person of ordinary skill in the art to modify and improve the Fleck reference in order to better meet its original objective of increased parallelism. There is no such thing as having too much speed, efficiency, or parallelism, which provides both. Therefore, this argument is not deemed persuasive.

28. In the remarks, Applicant argues on page 8, top paragraph, in substance that:

> "Specifically, this [Mukhanov] reference fails to disclose either a decoder that controls the channels or detects the type of the instructions, as set forth in independent claim 1."

This is not deemed persuasive because although Applicant is correct in stating that Mukhanov has not taught a decoder as claimed, the Rejection did not rely on it to do so. As noted above in the rejection of claim 1 and previous remarks, Fleck has taught a decoder that controls the channels and detects the type of the instructions.

29. In the remarks, Applicant argues on page 8, middle paragraph, in substance that:

> "Mohamed, however, teaches simultaneous execution of one single operation, and not of two independent operations within the functional units, as described in claim 8."

This is not deemed persuasive because although Applicant is correct in stating that Mohamed has not taught execution of two independent operations, the Rejection did not rely on it to do so. As noted above in the rejection of claim 8, Fleck has taught execution of two independent operations simultaneously by the two processing channels.

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephanie M. Deckter whose telephone number is 703-308-6132. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Stephanie M. Deckter
Examiner
Art Unit 2183 SMD

June 19, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100